| present application (claim 61) | '969 Patent (claims 1, 3, and 4) |
|---|---|
| An element substrate comprising: | A light emitting device comprising: (claim 1, ll. 1) |
| a first power line; a second power line; a scan line; a signal line; a pixel electrode; a first transistor; a second transistor; and a third transistor, | a scan line; a signal line intersecting with the scan line; a first to a n-th power supply lines ... a light emitting element; a first transistor ... a second transistor (claim 1, ll. 2-13) |
| wherein one of a source and a drain of the first transistor is connected to the pixel electrode, wherein one of a source and drain of the second transistor is connected to the other of the source and the drain of the first transistor, wherein the other of the source and the drain of the second transistor is connected to the first power line | wherein the first power source, the first transistor, the second transistor, and the light emitting element are connected in series (claim 1, ll. 14-16) |
| wherein a gate of the first transistor is connected to the second power line, | wherein a first region of a gate electrode of the first transistor is electrically connected to a k-th power supply line, wherein a second region of the gate electrode of the first transistor is electrically connected to a (k+1)-th power supply line (claim 1, ll. 17-22) |
| Limitation A | Limitation A' |

| | |
|---|---|
| wherein one of a source and a drain of the third transistor is connected to a gate electrode of the second transistor, wherein the other of the source and the drain of the third transistor is connected to the signal line, wherein a gate electrode of the third transistor is connected to the scan line, | |
| wherein the first transistor has a channel length longer than a channel width, and the second transistor has a channel length equal to or shorter than a channel width, and | wherein a channel length of the first transistor is longer than its channel width, and a channel length of the second transistor is equal to or shorter than its channel width (claim 3, ll. 1-5) |
| wherein a ratio of the channel length of the channel width of the first transistor is 5 or more. | a ratio of the channel length to the channel width of the first transistor is five or more (claim 4, ll. 1-3) |

The limitations of the '969 patent do not relate to each of the respective limitations of claim 61 as indicated in the mark-ups in the table above. For instance, claim 61 recites that one power supply line (i.e., in Limitation A - the second power supply line) is connected to the gate of the first transistor, whereas claims 1, 3 and 4 of the '969 patent recite that two power supply lines (i.e., in Limitation A' - the k-th and (k+1)-th power supply lines) are connected to the gate of the first transistor. Koyama fails to remedy the deficiencies of the '969 patent. For at least this reason, the rejection of claims 3, 36-38, 61 and 69, and their dependent claims, should be withdrawn.

Claims 3, 15, 17, 28, 32, 34-40, 43-47, 50-55, and 58-75 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 11, 14 and 15 of

Osame (U.S. Patent No. 7,141,934) in view of Koyama. Applicants request reconsideration and withdrawal of the rejection at least because the claims of Osame, even when considered in conjunction with Koyama, do not describe or suggest that "a gate electrode of the first transistor is connected to a second power line," as recited in claims 3 and 36-38, and "a gate electrode of the first transistor is connected to the second power line," as recited in claims 61 and 69.

A marked-up version of the table from the Office Action is shown below that compares the limitations of claim 61 of the current application with claims 11, 14 and 15 of Osame (the '934 patent). The marked-up version of the table below shows Limitations B and C in claim 61, and Limitations B' and C' in claims 11, 14 and 15 of the '934 patent.

| present application (claim 61) | '934 Patent (claims 11, 14, and 15) |
|---|---|
| An element substrate comprising: | A light emitting device comprising; (claim 11, l. 2) |
| a first power line; a second power line; a scan line; a signal line; a pixel electrode; a first transistor; a second transistor; and a third transistor, | a light emitting element provided in a pixel; a first transistor ... a second transistor ... a third transistor ...a first power supply and a second power supply (claim 11, ll. 2-12) |
| wherein one of a source and a drain of the first transistor is connected to the pixel electrode, wherein one of a source and drain of the second transistor is connected to the other of the source and the drain of the first transistor, wherein the other of the source and the drain of the second transistor is connected to the first power line Limitation B | wherein the light emitting element is connected in series to the first transistor and the second transistor between a first power supply and a second power supply (claim 11, ll. 10-12) Limitation B' |
| wherein a gate of the first transistor is connected to the second power line, Limitation C | a gate electrode of the first transistor is connected to the first power supply (claim 11, ll. 13-14) Limitation C' |
| wherein one of a source and a drain of the third transistor is connected to a gate electrode of the second transistor, wherein the other of the source and the drain of the third transistor is connected to the signal line, wherein a gate electrode of the third transistor is connected to the scan line, | |
| wherein the first transistor has a channel length longer than a channel width, and the second transistor has a channel length equal to or shorter than a channel width, and | wherein a channel length of the first transistor is longer than its channel width, and a channel length of the second transistor is equal to or shorter than its channel width (claim 14, ll. 1-4) |
| wherein a ratio of the channel length of the | a ratio of the channel length to the channel |
| channel width of the first transistor is 5 or more. | width of the first transistor is five or more (claim 15, ll. 1-3) |

As indicated in the Office Action, the Office relates limitation B in claim 61 to limitation B' in the '934 patent, and further relates limitation C to limitation C' in the '934 patent. However, if limitation C corresponds to the limitation C', limitation B does not correspond to the limitation B' because, as for

limitation B, the pixel electrode is **not** connected in series to the first transistor and the second transistor between the first power line and the second power line as recited in the '934 patent. For the sake of argument, even if the pixel electrode in the current application is connected in series to the first power line in claim 61, the pixel electrode is not located between the first power line and the second power line, as recited in the '934 patent, because claim 61 recites that the gate of the first transistor is connected to the second power line.

Similarly for claims 3, 36 and 37 of the current application, these claims recite that "the light-emitting element, the first transistor, and the second transistor are connected in series between a first power line and a counter electrode of the light-emitting element," and "a gate electrode of the first transistor is connected to a second power line." Hence, claims 3, 36 and 37 of the current application do not have limitations as asserted in the Office Action where the light emitting element is connected in series to the first transistor and the second transistor between a first power supply and a second power supply, as in claims 11, 14 and 15 of the '934 patent. Claims 38 and 69 of the current application recite limitations that are distinguished from claims 11, 14 and 15 of the '934 patent for similar reasons. Koyama does not remedy the above-described deficiencies of the '934 patent.

For at least these reasons, the rejection of claims 3, 36-38, 61 and 69, and their dependent claims, should be withdrawn.

All claims are in condition for allowance.

## ***Conclusion***

It is believed that all of the pending issues have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this reply should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this reply, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

No fee is believed due with this response. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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